EXHIBIT 1

JEDEC STANDARD

DDR5 SDRAM

JESD79-5A

(Revision of JESD79-5, JULY 2020)

October 2021

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

DDR5 SDRAM STANDARD

(From JEDEC Board Ballot JCB-21-31, formulated under the cognizance of the JC-42.3 Subcommittee on DRAM Memories.)

1 Scope

This document defines the DDR5 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 8Gb through 32Gb for x4, x8, and x16 DDR5 SDRAM devices. This standard was created based on the DDR4 standards (JESD79-4) and some aspects of the DDR, DDR2, DDR3 & LPDDR4 standards (JESD79, JESD79-2, JESD79-3 & JESD209-4).

1.1 JM7 Verbal Forms and Terms

JEDEC publication JM7 provides examples and directives for the use of verbal forms (e.g., 'shall' compared with 'should' and 'may' compared with 'can').'

This specification adheres to the verbal forms defined in JM7.01 July 2010 revision.

1.2 Significance of light grey Text in this Document

All light grey text is defined as something that should be considered TBD. The content may be accurate or the same as previous technologies but has not yet been reviewed or determined to be the working assumption.